IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Continuation of Serial No. 09/285,339

Applicant(s)	:	Seiji TANIZAWA et al.
For	:	EDITING SYSTEM AND METHOD AND DISTRIBUTION MEDIUM
Filed	:	Herewith
Examiner	:	C. Onuaku
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Charles Jackson
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PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Before the issuance of the first Office Action in the above-identified application, please amend the application as follows:

In the Specification:

Page 1, before line 2, please insert the following paragraph:

--This is a Continuation of Application Serial No. 09/285,339 filed April 2, 1999 now pending.--

Please replace the paragraph beginning at page 3, line 5, with the following rewritten paragraph:

--RAID-3 and RAID-5 are used most popularly for the general disk array unit out of these RAID levels. Fig. 82 show an exemplary structure of a RAID-3 type disk array unit, and Fig. 83 shows an exemplary structure of a RAID-5 type disk array unit.--

Please replace the paragraph beginning at page 3, line 10, with the following rewritten paragraph:

--In the RAID-3 type disk array unit shown in Fig. 82, the input data is divided in byte unit, and the data divided in byte unit are stored in a plurality of disk devices. The parity is stored in a pre-determined disk device as the error correction data. Herein, parities P1-4 corresponding to the data having the number 1 to 4 stored in a plurality of disk devices and parities P5-8 corresponding to the data having the number 5 to 8 are stored.--

Please replace the paragraph beginning at page 3, line 18, with the following rewritten paragraph:

--In the RAID-5 type disk array unit shown in Fig. 83, the input data is divided in sector unit, these data are interleaved and stored in a plurality of disk devices dispersedly. In this case,

data A, E, and I are stored in the first disk device, data B, F, and J are stored in the next disk device, data C, G, and parities PI-L corresponding to data I to L are stored in the next disk device. Data D, K, and parities PE-H corresponding to data E to H are stored in the next disk device, and parities PA-D corresponding to data A to D and data H and L are stored in the last disk device.--

Please replace the paragraph beginning at page 15, line 18, with the following rewritten paragraph:

--Fig. 1 shows an exemplary structure of an editing system to which the present invention is applied. In this system, the video data is supplied from a source video tape recorder (VTR) 9 and a daily server 7 to an editing system 1, and the video data is subjected to editing. The editing system 1 controls a disk recorder 2 to perform editing. The editing system 1 transmits the video data and audio data to the disk recorder 2 through a two channel SDI (Serial Data Interface), and the disk recorder 2 supplies 6 channel video data and 16 channel audio data to the editing system 1 through the SDI. Further, the editing system 1 supplies the audio data and video data to a main monitor 4, an on air buffer 8, the source VTR 9, a host personal computer 3 through the SDI. Further, the editing system 1 supplies the audio signal to an amplifier 5 to generate sound from a speaker 6.--

Please replace the paragraph beginning at page 16, line 16, with the following rewritten paragraph:

--Fig. 2 shows an exemplary internal structure of the editing system 1. The editing system 1 comprises a matrix switcher section 21 a video processing unit 22, an audio processing unit 23, and a system control section 24 connected to each other through a control bus 25.--

Please replace the paragraph beginning at page 16, line 21, with the following rewritten paragraph:

--As shown in Fig. 3, the system control section 24 is provided with a main CPU 121 for controlling the matrix switcher section 21, the video processing section 22, and the audio processing unit 23 through the control bus 25, and provided with device control CPU's 122-1 to 122-3 for controlling devices such as the source VTR 9, the disk recorder 2 served as a local storage, and daily server 7 through the control bus 25. Further, the system control section 24 is provided with a communication CPU 124 for operating interface processing for GUI and for operating input and output transmission of the reference time record between the host personal computer 3.--

Please replace the paragraph beginning at page 17, line 7, with the following rewritten paragraph:

--As shown in Fig. 4, the matrix switcher section 21 is a block for switching the input line and output line. The matrix switcher section 21 is provided with 12 input lines 31-1 to 31-12 for receiving the video signal or audio signal supplied based on the SDI format. 12 output lines corresponding to 12 input lines are disposed in the form of a matrix, each output line is provided with output processors 32-1 to 32-12. Input lines 31-1 to 31-12 and 12 output lines corresponding to the output processors 32-1 to 32-12 are connected at cross points marked with

X as required. The control block 34 of the matrix switcher section 21 receives a command from the main CPU 121 of the system control section 24 through the control bus 25, and the connection is controlled correspondingly to the command.--

Please replace the paragraph beginning at page 22, line 7, with the following rewritten paragraph:

--As shown in Fig. 6, in the audio processing unit 23, a separator block 81 is provided with separators 81-1 to 81-3, and these separators 81-1 to 81-3 separate an embedded audio signal from an SDI format signal supplied from the matrix switcher section 21. These signals are AES/EBU (Audio Engineering Society/European Broadcasting Union) format signals.--

Please replace the paragraph beginning at page 22, line 14, with the following rewritten paragraph:

--A mixer block 83 is provided with an adder 92-1 which adds the output of the separators 81-1 to 81-3 after the output is adjusted to a prescribed level by variable resistors 91-1 to 91-3, and provided with an adder 92-2 which adds the output of the separators 81-1 to 81-3 after the output is adjusted to a prescribed level by variable resistors 91-4 to 91-6.--

Please replace the paragraph beginning at page 23, line 14, with the following rewritten paragraph:

--In this exemplary structure, 32 hard disks 201-1 to 201-32 are provided, hard disks 201-1 to 201-28 out of these hard disks are served for video signal recording of RAID-5 system, on the other hand, hard disks 201-29 to 201-32 are served for audio signal recording of RAID-1

system. SCSI controllers 202-1 to 202-16 serve as SPCs (SCSI Peripheral Controller), respectively controlling two hard disks. For example, the SCSI controller 202-1 controls the hard disk 201-l and hard disk 201-2, SCSI controller 202-2 controls the hard disk 201-3 and hard disk 201-4.--

Please replace the paragraph beginning at page 26, line 15, with the following rewritten paragraph:

--The CPU block 261 is provided with the controller 262 and a RAM 263 and connected to the SCSI controller 202-i, the buffer block 203-i, the DMA controller 241, the input-output controller 242, the DMA controller 281-i, the RAID controller 282-i, the video processing section 283-i, and input output controller 284-i, and controls these components as required. The controller 262 controls blocks and the RAM 263 stores software programs and table data which are required for the controller 262 to operate various processing. The controller 262 generates and updates the determined format parameter and generates and updates a block map 304 based on the data from a zone bit recording (ZBR) table 301 formed in the RAM 263 as shown in Fig. 8. Herein, the format parameter comprises the size of one block of data S, the number of division of data n, and the optimal skew value θ skew.--

Please replace the paragraph beginning at page 29, line 19, with the following rewritten paragraph:

--Figs. 13A and 13B show an example of the physical address table 302. The logical sector number Lki is the number assigned sequentially to each sector of all the media in each hard disk 201-i, and as shown in Fig. 13A, the logical sector number Lki is specified by the

cylinder number CYLki, the medium number MEDki, and the sector number SECki. Fig. 13B shows a detailed example. For example, a sector corresponding to the logical sector number of 2 is the sector at the position of cylinder number 0, medium number 0, and sector number 2. Therefore, the logical sector number is converted to the physical sector number, or conversely, the physical sector number is converted to the logical sector number with reference to the physical address table 302.--

Please replace the paragraph beginning at page 36, line 26, with the following rewritten paragraph:

--As shown in Fig. 21, the time required for the head of the subblock to attain to the position under the head is obtained for each cylinder by the above-mentioned equation (2). However, because it is required for the head to attain to the desired cylinder within the time, the waiting time is the time from the seek to the time when the head of the block appears first. This time is the overhead Td (L) which involves both the seek and rotation waiting times. Fig. 22 shows an example, and the following equation represents the definition. The actual overhead (waiting time) Td (L) is shown with a thick line in Fig. 22. The function of the seek time Ts (L) is shown with a dashed line. In the drawing, Trot is 1 rotation period.--

Please replace the paragraph beginning at page 37, line 16, with the following rewritten paragraph:

--The subsequent steps S3-2, S3-3, and S3-4 are for selecting the skew θskew so that the straight line is always larger than the seek time Ts (L) and approximately touches the seek time Ts (L).--

Please replace the paragraph beginning at page 40, line 18, with the following rewritten paragraph:

--In the step S3 shown in Fig. 16, the skew θskew is selected so that the rotation waiting straight line given by the above-mentioned equation (2) lies above the seek time Ts (L) and nearest to the seek time Ts (L). Thereby, Td (L) is minimized at the vicinity of the distance La, and the resultant worst overhead Tmax is minimized.--

Please replace the paragraph beginning at page 40, line 24, with the following rewritten paragraph:

--Fig. 25 shows the length of overhead schematically in the case in which algorithm is used according to the above-mentioned method (FARAD system). As shown in Fig. 25, SCAN system in which a plurality of accesses is executed collectively from the outer circumference to the inner circumference in the order within the range of the collective accesses, or conversely, from the inner circumference to the outer circumference in the order to realize the shorter seek time in comparison with conventional system in which access is executed in the order of arising, and therefore the overhead can be the shorter. However, this SCAN system can shorten the seek time in comparison with the conventional system, but can not shorten the rotation waiting time. On the other hand, the above-mentioned method (FARAD system) can shorten not only the seek time as well as the SCAN system but also the rotation waiting time in comparison with the conventional system (SCAN system), and thus the total overhead can be shortened in comparison with SCAN system.--

Please replace the paragraph beginning at page 42, line 3, with the following rewritten paragraph:

--By applying the above-mentioned method, the overhead associated with migration between subblocks is improved greatly. However, in the case that the size of a subblock is large extending over a plurality of tracks and plurality of cylinders, the required time for changing track and migration time to the adjacent cylinder should be taken into consideration. Because the required time for changing track and migration to the adjacent cylinder are constant respectively, by giving skew between tracks and between cylinders so that the data arrives just under the head after the time, the long rotation waiting time in a subblock associated with changing track and migration to the adjacent cylinder is suppressed.--

Please replace the paragraph beginning at page 43, line 16, with the following rewritten paragraph:

--In the step S12-4, these re-arranged access requests are sent out to the hard disk 201 through the SCSI controller 202 in the order from the access request having the smallest cylinder number, and access and data transfer are operated actually. An access indication for one subblock is sent out, and after completion of data transfer in the step S12-6, then the next access indication is sent out. Whether transfer of all the requests is completed is determined in the step S12-6, if not all the requests are transferred, the sequence returns to the step S12-4, the same processing is operated. Such process is repeated N times, processing of the N access requests is determined to be completed in the step S12-6.--

Please replace the paragraph beginning at page 45, line 22, with the following rewritten paragraph:

--j = MOD (k-1, m) + 1 .... (4)--

Please replace the paragraph beginning at page 46, line 9, with the following rewritten paragraph:

--Thereby, for example, in the case of i=1 (the first subblock is recorded), hard disks 201 are selected in the order of j, such as 2, 3, 4, 5, ..., 32, 1, 2, ..., and in the case of i=3 (the third subblock is recorded), hard disks 201 are selected in the order such as 4, 5, 6, ..., 32, 1, 2, ...--

Please replace the paragraph beginning at page 46, line 19, with the following rewritten paragraph:

--Thereby, for example, in the case of i=2 (the second subblock is recorded), hard disks 201 of j= 3, 4, 5, ..., 32, 1, 2, ... are selected, and in the case of i=4 (the fourth subblock is recorded), hard disks 201 of j= 5, 6, 7, ..., 32, 1, 2, ... are selected sequentially.--

Please replace the paragraph beginning at page 49, line 14, with the following rewritten paragraph:

--Herein ROUNDUP represents an operator for calculating an integer which is obtained by rounding-up a fraction.--

Please replace the paragraph beginning at page 49, line 17, with the following rewritten paragraph:

--Next in the step S64, with reference to the physical address table 302 (Figs. 13A and 13B), the logical sector address (Lki) (in this case, Lkp) is determined from the physical sector address (CYLki, MEDki, SECki) calculated in the process of the steps S61 to S63, and the sequence proceeds to the return.--

Please replace the paragraph beginning at page 50, line 1, with the following rewritten paragraph:

--Fig. 31 is a flow chart for describing the detailed processing in the step S52 shown in Fig. 29. First in the step S71, the innermost circumferential track on the non-arranged areas is selected with reference to the physical address table 302 (Figs. 13A and 13B) as a track on which subblocks are arranged. Thereby, the cylinder number (CYLki) and medium number (MEDKi) of the physical sector address are determined, and the number of sectors (Tki) per 1 track at the map location is found with reference to the ZBR table 301.--

Please replace the paragraph beginning at page 50, line 10, with the following rewritten paragraph:

--Next in the step S72, an angle θki between the head of the innermost circumferential track on the non-arranged areas selected in the step S71 and the head of the physical innermost circumferential track (the track on which the data of the first subblock is recorded) is determined, and then the sector number (SECki) is determined in the step S73. In the step S74, the logical sector address (Lki) is determined based on the determined physical sector address (CYLki, MEDki, SECki), and the sequence proceeds to the return. The above-mentioned processing in steps S72 to S74 is basically the same as the processing in the steps S62 to S64 shown in Fig. 30

except that the track is selected sequentially from the inner circumference instead of the outer circumference, and the detailed description is omitted.--

Please replace the paragraph beginning at page 53, line 5, with the following rewritten paragraph:

--In the equation (11), MAX is an operator to determine the largest number of sectors among the size of subblocks Sk1 to Skn--

Please replace the paragraph beginning at page 54, line 19, with the following rewritten paragraph:

--After completion of the processing in the step S84, the sequence proceeds to the return. Thus, the processing of the step S33 in the flow chart shown in Fig. 27 is completed, and all the processes are completed.--

Please replace the paragraph beginning at page 54, line 23, with the following rewritten paragraph:

--As described herein above, the size of subblocks arranged on the inner circumference is made smaller and the size of subblocks arranged on the outer circumference is made larger so that the gap θgap of respective subblocks is equal to each other on respective hard disks 201.--

Please replace the paragraph beginning at page 59, line 16, with the following rewritten paragraph:

--The RAID controller 282-1 and the DMA controller 281-1 are connected to each other through FIFO's 404-1 to 406-1. The RAID controller 282-1 side of the FIFO's 404-1 to 406-1 is structured with a 32 bit bus, and the DMA controller 281-1 side is structured with a 64 bit bus. Because each FIFO has 32 bit structure, for example, the FIFO 404-1 delivers the 32 bit parity data supplied first to the DMA controller 281-1 through, for example, the higher 32 bit bus of the 64 bit bus, and supplies the next input 32 bit parity data to the DMA controller through the lower 32 bit bus of the 64 bit bus.--

Please replace the paragraph beginning at page 61, line 8, with the following rewritten paragraph:

--Though the drawing is omitted, also the SCSI boards 431-2 and 431-3 have the same structure as the SCSI board 431-1. Further, boards 421-2 and 421-3 also have the same structure as the board 421-1. Therefore, in this exemplary structure, one board 421-i can controls 12 hard disks 201, and actually 3 boards are provided, total 36 hard disks 201 can be controlled However, actually 32 hard disks 201 are connected.--

Please replace the paragraph beginning at page 66, line 8, with the following rewritten paragraph:

--On the other hand, the DMA command shown in the right side of Fig. 44 is served to DMA-transfer packet transfer blocks on 2:1 RAID area to the data buffer 212. In detail, the packet transfer block An+1 of the first subblock is stored in the address a0 of the data buffer 212. Similarly, the packet transfer block Cn+1 of the third subblock is stored in the address c0 of the data buffer 212, and the parity data Pn+1 is stored in the address p0 of the data buffer 212.

Similarly in the following, the second and following packet transfer blocks An+2, Cn+2, Pn+2, An+3, Cn+3, Pn+3, ... are transferred sequentially. When, the number of transferring of the packet transfer block is r-n+2.--

Please replace the paragraph beginning at page 66, line 20, with the following rewritten paragraph:

--Fig. 45 and Fig. 46 shows the DMA command for reading out the packet transfer block from the data buffer 212. Fig. 45 shows the case where there are no errors in the packet transfer blocks, and Fig. 46 shows the case where there are some errors.--

Please replace the paragraph beginning at page 66, line 24, with the following rewritten paragraph:

--As shown in Fig. 45, in the case where there are no errors in the packet transfer blocks, addresses a0 to d0 of the data buffer 212 in which each packet transfer block is stored and the number of transferring are written. In detail, in this case, one packet transfer block of the first subblock is read out from the address a0 of the data buffer 212, one packet transfer block of the second subblock is read out from the address b0, one packet transfer block of the third subblock is read out from the address c0, and one packet transfer block of the fourth subblock is read out from the address d0. Such reading out operation is repeated the number of times equivalent to the number of loops.--

Please replace the paragraph beginning at page 70, line 19, with the following rewritten paragraph:

--Similarly in the following, as shown in Fig. 48, when the packet transfer block of number 2 is supplied to the selector 451, the selector 455 calculates and delivers the exclusive OR of packet transfer blocks of number 0, number 1, and number 2, and further when the packet transfer block of number 3 is entered, the exclusive OR of packet transfer blocks of number 0 to number 3 is calculated and delivered. In the case of 4:1 RAID, this output is the parity to be obtained.--

Please replace the paragraph beginning at page 71, line 24, with the following rewritten paragraph:

--The SCSI controller 202 receives supply of a command from the controller 262 through the control bus 252, delivers a control signal to the buffer controller 211 corresponding to the command, and reproduces the pixel data and the parity data stored in the data buffer 212 and takes it in. The SCSI controller 202 writes the data taken in from the data buffer 212 through the buffer controller 211 on the prescribed track of the corresponding prescribed hard disk 201. As described herein above, the pixel data of 1 frame, which is divided into 4 subblocks, is recorded in different hard disks 201 for respective subblocks, for example, as shown in Fig. 33. The parity data corresponding to the pixel data of this frame is recorded in a different hard disk 201.--

Please replace the paragraph beginning at page 72, line 11, with the following rewritten paragraph:

--Next, the operation in which an error of the data reproduced from the hard disk 201 is corrected and the corrected data sent out is described with reference to Fig. 49. The controller 262 delivers a command to the SCSI controller 202 through the control bus 252 to reproduce the

parity data corresponding to the pixel data of a prescribed frame recorded in the hard disk 201. The reproduced data is written on the data buffer 212 from the SCSI controller 202 through the buffer controller 211. The controller 262 indicates to the DMA controller 281 through the control bus 252 to perform DMA transfer of the data written in the data buffer 212 as described herein above to the RAID controller 282. The DMA controller 281 reads out the data written on the data buffer 212 through the buffer controller 211 corresponding to the command, and receives the transfer through the DMA bus 251. The data is supplied to and stored in the FIFO 406A-1 and 406B-1 through the 64 bit bus. The data written on the FIFO 406A-1 and 406B-1 is supplied to the RAID controller 282 through the 32 bit bus.--

Please replace the paragraph beginning at page 83, line 23, with the following rewritten paragraph:

--In the range T1, transfer is performed corresponding to the DMA command which indicates 4:1 RAID. In this case, the video data (50304 word pixel data) of 393 packet transfer blocks of the first to fourth subblock is DMA-transferred to and written in the second to fifth addresses of the data buffer 201 corresponding to the hard disks 201-2 to 201-5 having disk ID of 2 to 5. Further, the parity data (50304 word parity data) of 393 packet transfer blocks is stored in the first address of the data buffer 212 corresponding to the hard disk 201-1 having disk ID of 1 by way of 393 loop transfers.

Please replace the paragraph beginning at page 84, line 8, with the following rewritten paragraph:

--Next, the DMA controller 281 writes the pixel data of 174 sectors corresponding to the range T2 of the second subblock in the seventh address (the address next to the area where the pixel data of 393 sectors of the second subblock in the range T1 is recorded) of the hard disk 201-3 having disk ID of 3 by way of 174 loop transfers corresponding to the DMA command of 2 : 1 RAID. Further similarly, the DMA controller 281 transfers to and writes in the eight address (the address next to the area where the video data of 393 sectors of the fourth subblock in the range T1 is recorded) of the data buffer 212 corresponding to the hard disk 201-5 having hard disk ID of 5 by way of 174 loop transfers. Further, the parity data (22272 word parity data) of the 174 packet transfer blocks is written in the sixth address (the address next to the area where the parity data of 393 sectors in the range T1 is recorded) corresponding to the hard disk 201 having disk ID of 1.--

Please replace the paragraph beginning at page 94, line 23, with the following rewritten paragraph:

--When a prescribed command is entered from the host personal computer 3 in the matrix switcher section 21, the video signal processed in the video processing section 22 is selected properly, and supplies to any one of output processors 32-3 to 32-12, further supplied from any one of the combiners 33-1 to 33-10 to the disk recorder 2, and written in the hard disk 201.--

In the Claims:

Please cancel claims 1-18.

Please amend claims 19-21 by rewriting the same as follows:

--19. (Amended) An editing system comprising:

storing means for storing audio data to be reproduced;

synthesizing means for synthesizing a plurality of channels of said audio data;

changing means for changing the reproduction speed of said audio data without affecting an interval thereof; and

supplying means for supplying the audio data synthesized by said synthesizing means and the audio data whose reproduction speed is changed by said changing means to arbitrary output channels,

wherein said changing means changes the reproduction speed of said audio data without changing the pitch.

20. (Amended) An editing method comprising:

a storing step of storing audio data to be reproduced;

a synthesizing step of synthesizing said audio data of a plurality of channels;

a changing step of changing the reproduction speed of said audio data without affecting an interval thereof; and

a supplying step of supplying the audio data synthesized in said synthesizing step and the audio data whose reproduction speed is changed in said changing step to arbitrary output channels,

wherein said changing step changes the reproduction speed of said audio data without changing the pitch.

21. (Amended) A distribution medium for providing a program which controls an editing system to perform a process comprising:

a storing step of storing audio data to be reproduced;

a synthesizing step of synthesizing said audio data of a plurality of channels;

a changing step of changing the reproduction speed of said audio data without affecting an interval thereof; and

a supplying step of supplying the audio data synthesized in said synthesizing step and the audio data whose reproduction speed is changed in said changing step to arbitrary output channels,

wherein said changing step changes the reproduction speed of said audio data without changing the pitch.--

REMARKS

Applicants enclose a Request for Approval of Drawing Changes that corrects Figs. 7, 11B, 16, 18, 20, 33, 48, 54, and 62B to be consistent with the specification.

Applicants have amended the specification to correct minor typographical errors. Claims 19-21 are presented to continue prosecution of aspects of Applicants' invention. Applicants have cancelled claims 1-18.

Applicants have amended claims 19-21 for clarification. Attached hereto is a marked-up version of the changes made to the specification and the claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."** It is submitted that these claims, as originally presented, are patentable, and that these claims were in full compliance with the requirements of 35 USC 112. Changes to these claims, as presented herein, are not made for the purpose of patentability within the meaning of 35 USC sections 101, 102, 103 or 112. Rather, these changes are made simply for clarification and to round out the scope

of protection to which Applicants are entitled. The features defined by the presented claims are fully disclosed in the specification and drawings as originally filed. No new matter is presented.

The Examiner is hereby authorized to charge any insufficient fees or credit any overpayment associated with the above-identified application to Deposit Account No. 50-0320.

An early examination on the merits is solicited.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP

By: [signature]
William S. Frommer
Reg. No. 25,506
(212) 588-0800

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Page 1, before line 2, please insert the following paragraph:

--This is a Continuation of Application Serial No. 09/285,339 filed April 2, 1999 now pending.--

Please replace the paragraph beginning at page 3, line 5, with the following rewritten paragraph:

--RAID-3 and RAID-5 are used most popularly for the general disk array unit out of these RAID levels. [Figs. 75A to 75C] Fig. 82 show an exemplary structure of a RAID-3 type disk array unit, and Fig. [76] 83 shows an exemplary structure of a RAID-5 type disk array unit.--

Please replace the paragraph beginning at page 3, line 10, with the following rewritten paragraph:

--In the RAID-3 type disk array unit shown in [Figs. 75A to 75C] Fig. 82, the input data is divided in byte unit, and the data divided in byte unit are stored in a plurality of disk devices. The parity is stored in a pre-determined disk device as the error correction data. Herein, parities P1-4 corresponding to the data having the number 1 to 4 stored in a plurality of disk devices and parities P5-8 corresponding to the data having the number 5 to 8 are stored.--

Please replace the paragraph beginning at page 3, line 18, with the following rewritten paragraph:

--In the RAID-5 type disk array unit shown in Fig. [76] 83, the input data is divided in sector unit, these data are interleaved and stored in a plurality of disk devices dispersedly. In this case, data A, E, and I are stored in the first disk device, data B, F, and J are stored in the next disk device, data C, G, and parities PI-L corresponding to data I to L are stored in the next disk device. Data D, K, and parities PE-H corresponding to data E to H are stored in the next disk device, and parities PA-D corresponding to data A to D and data H and L are stored in the last disk device.--

Please replace the paragraph beginning at page 15, line 18, with the following rewritten paragraph:

--Fig. 1 shows an exemplary structure of an editing system to which the present invention is applied. In this system, the video data is supplied from a source video tape recorder (VTR) 9 and a daily server 7 to an editing system 1, and the video data is subjected to editing. The editing system 1 controls a disk recorder 2 to perform editing. The editing system 1 transmits the video data and audio data to the disk recorder 2 through a two channel SDI (Serial Data Interface), and the disk recorder 2 supplies 6 channel video data and 16 channel audio data to the editing system 1 [though] through the SDI. Further, the editing system 1 supplies the audio data and video data to a main monitor 4, an on air buffer 8, the source VTR 9, a host personal computer 3 through the SDI. Further, the editing system 1 supplies the audio signal to an amplifier 5 to generate sound from a speaker 6.--

Please replace the paragraph beginning at page 16, line 16, with the following rewritten paragraph:

--Fig. 2 shows an exemplary internal structure of the editing system 1. The editing system 1 comprises a matrix switcher section 21 a video processing unit 22, an audio processing unit 23, and a system control section 24 connected to each other through a control bus 25[, a video processing unit 22, an audio processing unit 23, and a system control section 24].--

Please replace the paragraph beginning at page 16, line 21, with the following rewritten paragraph:

--As shown in Fig. 3, the system control section 24 is provided with a main CPU 121 for controlling the matrix switcher section 21, the video processing section 22, and the audio processing unit 23 through [a] the control bus 25, and provided with [a] device control CPU's 122-1 to 122-3 for controlling devices such as the source VTR 9, the disk recorder 2 served as a local storage, and daily server 7 through the control bus 25. Further, the system control section 24 is provided with a communication CPU 124 for operating interface processing for GUI and for operating input and output transmission of the reference time record between the host personal computer 3.--

Please replace the paragraph beginning at page 17, line 7, with the following rewritten paragraph:

--As shown in Fig. 4, the matrix switcher section 21 is a block for switching the input line and output line. The matrix switcher section 21 is provided with 12 input lines 31-1 to 31-12 for receiving the video signal or audio signal supplied based on the SDI format. 12 output lines corresponding to 12 input lines are disposed in the form of a matrix, each output line is provided with output processors 32-1 to 32-12. Input lines 31-1 to 31-12 and 12 output lines

corresponding to the output processors 32-1 to 32-12 are connected at cross points marked with X as required. The control block 34 of the matrix switcher section 21 receives a command from the main CPU 121 of the system control section 24 through the control bus 25, and the connection is controlled correspondingly to the command.--

Please replace the paragraph beginning at page 22, line 7, with the following rewritten paragraph:

--As shown in Fig. 6, in the audio processing unit 23, a separator block 81 is provided with separators 81-1 to 81-3, and these separators 81-1 to 81-3 separate an embedded audio signal from an SDI format signal supplied from the matrix switcher section 21. These signals are AES/EBU (Audio Engineering Society/European Broadcasting Union) format signals.--

Please replace the paragraph beginning at page 22, line 14, with the following rewritten paragraph:

--A mixer block 83 is provided with an adder 92-1 which adds the output of the separators 81-1 to 81-3 after the output is adjusted to a prescribed level by variable resistors [92-1to 92-3] 91-1 to 91-3, and provided with an adder 92-2 which adds the output of the separators 81-1 to 81-3 after the output is adjusted to a prescribed level by variable resistors 91-4 to 91-6.--

Please replace the paragraph beginning at page 23, line 14, with the following rewritten paragraph:

--In this exemplary structure, 32 hard disks 201-1 to 201-32 are provided, hard disks 201-1 to 201-28 out of these hard disks are served for video signal recording of RAID-5 system, on the other hand, hard disks 201-29 to 201-32 are served for audio signal recording of RAID-1 system. SCSI controllers 202-1 to 202-16 [served as SPC] serve as SPCs (SCSI Peripheral Controller), respectively controlling two hard disks. For example, the SCSI controller [201-1] 202-1 controls the hard disk 201-l and hard disk 201-2, SCSI controller [201-2] 202-2 controls the hard disk 201-3 and hard disk 201-4.--

Please replace the paragraph beginning at page 26, line 15, with the following rewritten paragraph:

--The CPU block 261 is provided with the controller 262 and a RAM 263 and connected to the SCSI controller 202-i, the buffer block 203-i, the DMA controller 241[-i], the input-output controller 242[-i], the DMA controller 281-i, the RAID controller 282-i, the video processing section [282-i] 283-i, and input output controller 284-i, and controls these components as required. The controller 262 controls blocks and the RAM 263 stores software programs and table data which are required for the controller 262 to operate various processing. The controller 262 generates and updates the determined format parameter and generates and updates a block map 304 based on the data from a zone bit recording (ZBR) table 301 formed in the RAM 263 as shown in Fig. 8. Herein, the format parameter comprises the size of one block of data S, the number of division of data n, and the optimal skew value θ skew.--

Please replace the paragraph beginning at page 29, line 19, with the following rewritten paragraph:

--Figs. 13A and 13B show an example of the physical address table 302. The logical sector number Lki is the number assigned sequentially to each sector of all the media in each hard disk 201-i, and as shown in Fig. [9 (A)] 13A, the logical sector number Lki is specified by the cylinder number CYLki, the medium number MEDki, and the sector number SECki. Fig. [9(b)] 13B shows a detailed example. For example, a sector corresponding to the logical sector number of 2 is the sector at the position of cylinder number 0, medium number 0, and sector number 2. Therefore, the logical sector number is converted to the physical sector number, or conversely, the physical sector number is converted to the logical sector number with reference to the physical address table 302.--

Please replace the paragraph beginning at page 36, line 26, with the following rewritten paragraph:

--As shown in Fig. 21, the time required for the head of the subblock to attain to the position under the head is obtained for each cylinder by the above-mentioned equation (2). However, because it is required for the head to attain to the desired cylinder within the time, the waiting time is the time from the seek to the time when the head of the block appears first. This time is the overhead Td (L) which involves both the seek and rotation waiting [both] times. Fig. 22 shows an example, and the following equation represents the definition. The actual overhead (waiting time) Td (L) is shown with a thick line in Fig. 22. The function of the seek time Ts (L) is shown with a dashed line. In the drawing, Trot is 1 rotation period.--

Please replace the paragraph beginning at page 37, line 16, with the following rewritten paragraph:

--The subsequent steps S3-2, S3-3, and S3-4 [is the step] are for selecting the skew θskew so that the straight line is always larger than the seek time Ts (L) and approximately touches the seek time Ts (L).--

Please replace the paragraph beginning at page 40, line 18, with the following rewritten paragraph:

--In the step S3 shown in Fig. 16, the skew θskew is selected so that the rotation waiting straight line[s] given by the above-mentioned equation (2) lies above the seek time Ts (L) and nearest to the seek time Ts (L). Thereby, Td (L) is minimized at the vicinity of the distance La, and the resultant worst overhead Tmax is minimized.--

Please replace the paragraph beginning at page 40, line 24, with the following rewritten paragraph:

--Fig. 25 shows the length of overhead schematically in the case in which algorithm is used according to the above-mentioned method (FARAD system). As shown in Fig. 25, SCAN system in which a plurality of accesses is executed collectively from the outer circumference to the inner circumference in the order within the range of [collected assesses] the collective accesses, or conversely, from the inner circumference to the outer circumference in the order [can] to realize the shorter seek time in comparison with conventional system in which access is executed in the order of arising, and therefore the overhead can be the shorter. However, this SCAN system can shorten the seek time in comparison with the conventional system, but can not shorten the rotation waiting time. On the other hand, the above-mentioned method (FARAD system) can shorten not only the seek time as well as the SCAN system but also the rotation

waiting time in comparison with the conventional system (SCAN system), and thus the total overhead can be shortened in comparison with SCAN system.--

Please replace the paragraph beginning at page 42, line 3, with the following rewritten paragraph:

--By applying the above-mentioned method, the overhead associated with migration between subblocks is improved greatly. However, in the case that the size of a subblock is large extending over a plurality of tracks and plurality of cylinders, the required time for changing track and migration time to the adjacent cylinder should be taken into consideration. Because the required time for changing track and migration to the adjacent cylinder are constant respectively, by giving skew between tracks and between cylinders so that the data arrives just under the head after the time, the long rotation waiting time in a subblock associated with changing track and migration to the adjacent cylinder is suppressed.--

Please replace the paragraph beginning at page 43, line 16, with the following rewritten paragraph:

--In the step S12-4, these re-arranged [these] access requests are sent out to the hard disk 201 through the SCSI controller 202 in the order from the access request having the smallest cylinder number, and access and data transfer are operated actually. An access indication for one subblock is sent out, and after completion of data transfer in the step S12-6, then the next access indication is sent out. Whether transfer of all the requests is completed is determined in the step S12-6, if not all the requests are transferred, the sequence returns to the step S12-4, the same

processing is operated. Such process is repeated N times, processing of the N access requests is determined to be completed in the step S12-6.--

Please replace the paragraph beginning at page 45, line 22, with the following rewritten paragraph:

--j = MOD (k-1[)], m) + 1 .... (4)--

Please replace the paragraph beginning at page 46, line 9, with the following rewritten paragraph:

--Thereby, for example, in the case of i=1 (the first subblock is recorded), hard disks 201 are selected in the order of j, such as 2, 3, 4, 5, ..., 32, 1, 2, ..., and in the case of i=3 (the third subblock is recorded), hard disks 201 are selected in the order such as 4, 5, 6, ..., 32, 1, 2, ...--

Please replace the paragraph beginning at page 46, line 19, with the following rewritten paragraph:

--Thereby, for example, in the case of i=2 (the second subblock is recorded), hard disks 201 of j= 3, 4, 5, ..., 32, 1, 2, ... are selected, and in the case of i=4 (the fourth subblock is recorded), hard disks 201 of j= 5, 6, 7, ..., 32, 1, 2, ... are selected sequentially.--

Please replace the paragraph beginning at page 49, line 14, with the following rewritten paragraph:

--Herein ROUNDUP represents an operator for calculating an integer which is obtained by rounding-up [of] a fraction.--

Please replace the paragraph beginning at page 49, line 17, with the following rewritten paragraph:

--Next in the step S64, with reference to the physical address table 302 (Figs. 13A and 13B), the logical sector address ([lki] Lki) (in this case, Lkp) is determined from the physical sector address (CYLki, MEDki, SECki) calculated in the process of the steps S61 to S63, and the sequence proceeds to the return.--

Please replace the paragraph beginning at page 50, line 1, with the following rewritten paragraph:

--Fig. 31 is a flow chart for describing the detailed processing in the step S52 shown in Fig. 29. First in the step S71, the innermost circumferential track on the non-arranged areas is selected with reference to the physical address table 302 (Figs. 13A and 13B) as a track on which subblocks are arranged. Thereby, the cylinder number (CYLki) and medium number ([MEKki] MEDKi) of the physical sector address are determined, and the number of sectors (Tki) per 1 track at the map location is found with reference to the ZBR table 301.--

Please replace the paragraph beginning at page 50, line 10, with the following rewritten paragraph:

--Next in the step S72, an angle θki between the head of the innermost circumferential track on the non-arranged areas selected in the step S71 and the head of the physical innermost

circumferential track (the track on which the data of the first subblock is recorded) is determined, and then the sector number (SECki) is determined in the step S73. In the step S74, the logical sector address (Lki) is determined based on the determined physical sector address (CYLki, MEDki, SECki), and the sequence proceeds to the return. The above-mentioned processing in steps S72 to S74 is basically the same as the processing in the steps S62 to S64 shown in Fig. 30 except[ing] that the track is selected sequentially from the inner circumference instead of the outer circumference, and the detailed description is omitted.--

Please replace the paragraph beginning at page 53, line 5, with the following rewritten paragraph:

--In the equation (11), MAX is an operator to determine the largest number of sectors among the size of subblocks [Ski] Sk1 to Skn--

Please replace the paragraph beginning at page 54, line 19, with the following rewritten paragraph:

--After completion of the processing in the step S84, the sequence proceeds to the return. Thus, the processing of the step S33 in the flow chart shown in Fig. [23] 27 is completed, and all the processes are completed.--

Please replace the paragraph beginning at page 54, line 23, with the following rewritten paragraph:

--As described herein above, the size of subblocks arranged on the inner circumference is made smaller and the size of subblocks arranged on the outer circumference is made larger so that the gap θgap of respective subblocks is equal to each other on respective hard disks 201.--

Please replace the paragraph beginning at page 59, line 16, with the following rewritten paragraph:

--The RAID controller 282-1 and the DMA controller 281-1 are connected to each other through FIFO's 404-1 to 406-1. The RAID controller 282-1 side of the FIFO's 404-1 to 406-1 is structured with a 32 bit bus, and the DMA controller 281-1 side is structured with a 64 bit bus. Because each FIFO has 32 bit structure, for example, the FIFO 404-1 delivers the 32 bit parity data supplied first to the DMA controller 281-1 through, for example, the higher 32 bit bus of the 64 bit bus, and supplies the next input 32 bit parity data to the DMA controller through the lower 32 bit bus of the 64 bit bus.--

Please replace the paragraph beginning at page 61, line 8, with the following rewritten paragraph:

--Though the drawing is omitted, also the SCSI boards 431-2 and 431-3 have the same structure as the SCSI board 431-1. Further, boards 421-2 and [431-3] 421-3 also have the same structure as the board 421-1. Therefore, in this exemplary structure, one board 421-i can controls 12 hard disks 201, and actually 3 boards are provided, total 36 hard disks 201 can be controlled However, actually 32 hard disks 201 are connected.--

Please replace the paragraph beginning at page 66, line 8, with the following rewritten

paragraph:

--On the other hand, the DMA command shown in the right side of Fig. 44 is served to DMA-transfer packet transfer blocks on 2:1 RAID area to the data buffer 212. In detail, the packet transfer block An+1 of the first subblock is stored in the address a0 of the data buffer 212. Similarly, the packet transfer block Cn+1 of the third subblock is stored in the address c0 of the data buffer 212, and the parity data Pn+1 is stored in the address p0 of the data buffer 212. Similarly in the following, the second and following packet transfer blocks An+2, [Cn+3] Cn+2, Pn+2, An+3, Cn+3, [+n+3] Pn+3, ... are transferred sequentially. When, the number of transferring of the packet transfer block is r-n+2.--

Please replace the paragraph beginning at page 66, line 20, with the following rewritten paragraph:

--Fig. 45 and Fig. 46 shows the DMA command for reading out the packet transfer block from the data buffer 212. Fig. 45 shows the case [that] where there [is] are no errors in the packet transfer blocks, and Fig. 46 shows the case [that] where there [is] are some errors.--

Please replace the paragraph beginning at page 66, line 24, with the following rewritten paragraph:

--As shown in Fig. 45, in the [cast that] case where there [is] are no errors in the packet transfer blocks, addresses a0 to d0 of the data buffer 212 in which each packet transfer block is stored and the number of transferring are written. In detail, in this case, one packet transfer block of the first subblock is read out from the address a0 of the data buffer 212, one packet transfer block of the second subblock is read out from the address b0, one packet transfer block

of the third subblock is read out from the address c0, and one packet transfer block of the fourth subblock is read out from the address d0. Such reading out operation is repeated the number of times equivalent to the number of loops.--

Please replace the paragraph beginning at page 70, line 19, with the following rewritten paragraph:

--Similarly in the following, as shown in Fig. 48, when the packet transfer block of number 2 is supplied to the selector 451, the selector 455 calculates and delivers the exclusive OR of packet transfer blocks of number 0, number 1, and number [3] 2, and further when the packet transfer block of number 3 is entered, the exclusive OR of packet transfer blocks of number 0 to number 3 is calculated and delivered. In the case of 4:1 RAID, this output is the parity to be obtained.--

Please replace the paragraph beginning at page 71, line 24, with the following rewritten paragraph:

--The SCSI controller 202 receives supply of a command from the controller 262 through the control bus 252, delivers a control[s] signal to the buffer controller 211 corresponding[ly] to the command, and reproduces the pixel data and the parity data stored in the data buffer 212 and takes it in. The SCSI controller 202 writes the data taken in from the data buffer 212 through the buffer controller 211 on the prescribed track of the corresponding prescribed hard disk 201. As described herein above, the pixel data of 1 frame, which is divided into 4 subblocks, is recorded in different hard disks 201 for respective subblocks, for example, as shown in Fig. 33. The parity data corresponding to the pixel data of this frame is recorded in a different hard disk 201.--

Please replace the paragraph beginning at page 72, line 11, with the following rewritten paragraph:

--Next, the operation in which an error of the data reproduced from the hard disk 201 is corrected and the corrected data [is] sent out is described with reference to Fig. 49. The controller 262 delivers a command to the SCSI controller 202 through the control bus 252 to reproduce the parity data corresponding to the pixel data of a prescribed frame recorded in the hard disk 201. The reproduced data is written on the data buffer 212 from the SCSI controller 202 through the buffer controller 211. The controller 262 indicates to the DMA controller 281 through the control bus 252 to perform DMA transfer of the data written in the data buffer 212 as described herein above to the RAID controller 282. The DMA controller 281 reads out the data written on the data buffer 212 through the buffer controller 211 corresponding[ly] to the command, and receives the transfer through the DMA bus 251. The data is supplied to and stored in the FIFO 406A-1 and 406B-1 through the 64 bit bus. The data written on the FIFO 406A-1 and 406B-1 is supplied to the RAID controller 282 through the 32 bit bus.--

Please replace the paragraph beginning at page 83, line 23, with the following rewritten paragraph:

--In the range T1, transfer is performed corresponding[ly] to the DMA command which indicates 4:1 RAID. In this case, the video data (50304 word pixel data) of 393 packet transfer blocks of the first to fourth subblock is DMA-transferred to and written in the second to fifth addresses of the data buffer 201 corresponding to the hard disks 201-2 to 201-5 having disk ID of 2 to 5. Further, the parity data (50304 word parity data) of 393 packet transfer blocks is stored

in the first address of the data buffer 212 corresponding to the hard disk 201-1 having disk ID of 1 by way of 393 loop transfers.

Please replace the paragraph beginning at page 84, line 8, with the following rewritten paragraph:

--Next, the DMA controller 281 writes the pixel data of 174 sectors corresponding to the range T2 of the second subblock in the seventh address (the address next to the area where the pixel data of 393 sectors of the second subblock in the range T1 is recorded) of the hard disk 201-3 having disk ID of 3 by way of 174 loop transfers corresponding[ly] to the DMA command of 2 : 1 RAID. Further similarly, the DMA controller 281 transfers to and writes in the eight address (the address next to the area where the video data of 393 sectors of the fourth subblock in the range T1 is recorded) of the data buffer 212 corresponding to the hard disk 201-5 having hard disk ID of 5 by way of 174 loop transfers. Further, the parity data (22272 word parity data) of the 174 packet transfer blocks is written in the sixth address (the address next to the area where the parity data of 393 sectors in the range T1 is recorded) corresponding to the hard disk 201 having disk ID of 1.--

Please replace the paragraph beginning at page 94, line 23, with the following rewritten paragraph:

--When a prescribed command is entered from the host personal computer 3 in the matrix switcher section 21, the video signal processed in the video processing section 22 is selected properly, and supplies to any one of output processors [21-3] 32-3 to 32-12, further supplied

from any one of the combiners 33-1 to 33-10 to the disk recorder 2, and written in the hard disk 201.--

In the Claims:

Please cancel claims 1-18.

Please amend claims 19-21 by rewriting the same as follows:

--19. (Amended) An editing system [as claimed in claim 18] comprising:

storing means for storing audio data to be reproduced;

synthesizing means for synthesizing a plurality of channels of said audio data;

changing means for changing the reproduction speed of said audio data without affecting an interval thereof; and

supplying means for supplying the audio data synthesized by said synthesizing means and the audio data whose reproduction speed is changed by said changing means to arbitrary output channels,

wherein said changing means changes the reproduction speed of said audio data without changing the pitch.

20. (Amended) An editing method comprising:

a storing step of storing [said] audio data to be reproduced;

a synthesizing step of synthesizing said audio data of a plurality of channels;

a changing step of changing the reproduction speed of said audio data without affecting an interval thereof; and

a supplying step of supplying the audio data synthesized in said synthesizing step and the audio data whose reproduction speed is changed in said changing step to arbitrary output channels,

wherein said changing step changes the reproduction speed of said audio data without changing the pitch.

21. (Amended) A distribution medium for providing a program which controls an editing system to perform a process comprising:

a storing step of storing [said] audio data to be reproduced;

a synthesizing step of synthesizing said audio data of a plurality of channels;

a changing step of changing the reproduction speed of said audio data without affecting an interval thereof; and

a supplying step of supplying the audio data synthesized in said synthesizing step and the audio data whose reproduction speed is changed in said changing step to arbitrary output channels,

wherein said changing step changes the reproduction speed of said audio data without changing the pitch.--

PATENT
450100-4830.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Continuation of Serial No. 09/285,339

Applicant(s)	:	Seiji TANIZAWA et al.
For	:	EDITING SYSTEM AND METHOD AND DISTRIBUTION MEDIUM
Filed	:	Herewith
Examiner	:	C. Onuaku
Art Unit	:	2615

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New York, NY 10151
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Date of Deposit: November 14, 2001

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Charles Jackson
(Typed or printed name of person mailing paper or fee)

Charles Jackson
(Signature of person mailing paper or fee)

REQUEST FOR APPROVAL OF DRAWING CHANGES

Assistant Commissioner for Patents
Washington, D.C. 20231

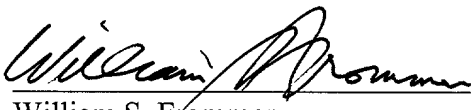
Attention: Official Draftsperson

Sir:

The undersigned attorney respectfully requests approval of changes to drawing Figs. 7, 11B, 16, 18, 20, 33, 48, 54, and 62B in the above-referenced application. The changes

are indicated in red ink on the accompanying photocopies and have been incorporated into the formal drawings filed herewith.

Respectfully submitted,
FROMMER LAWRENCE & HAUG LLP
Attorneys for Applicant



William S. Frommer
Registration No. 25,506
(212) 588-0800

FIG. 7

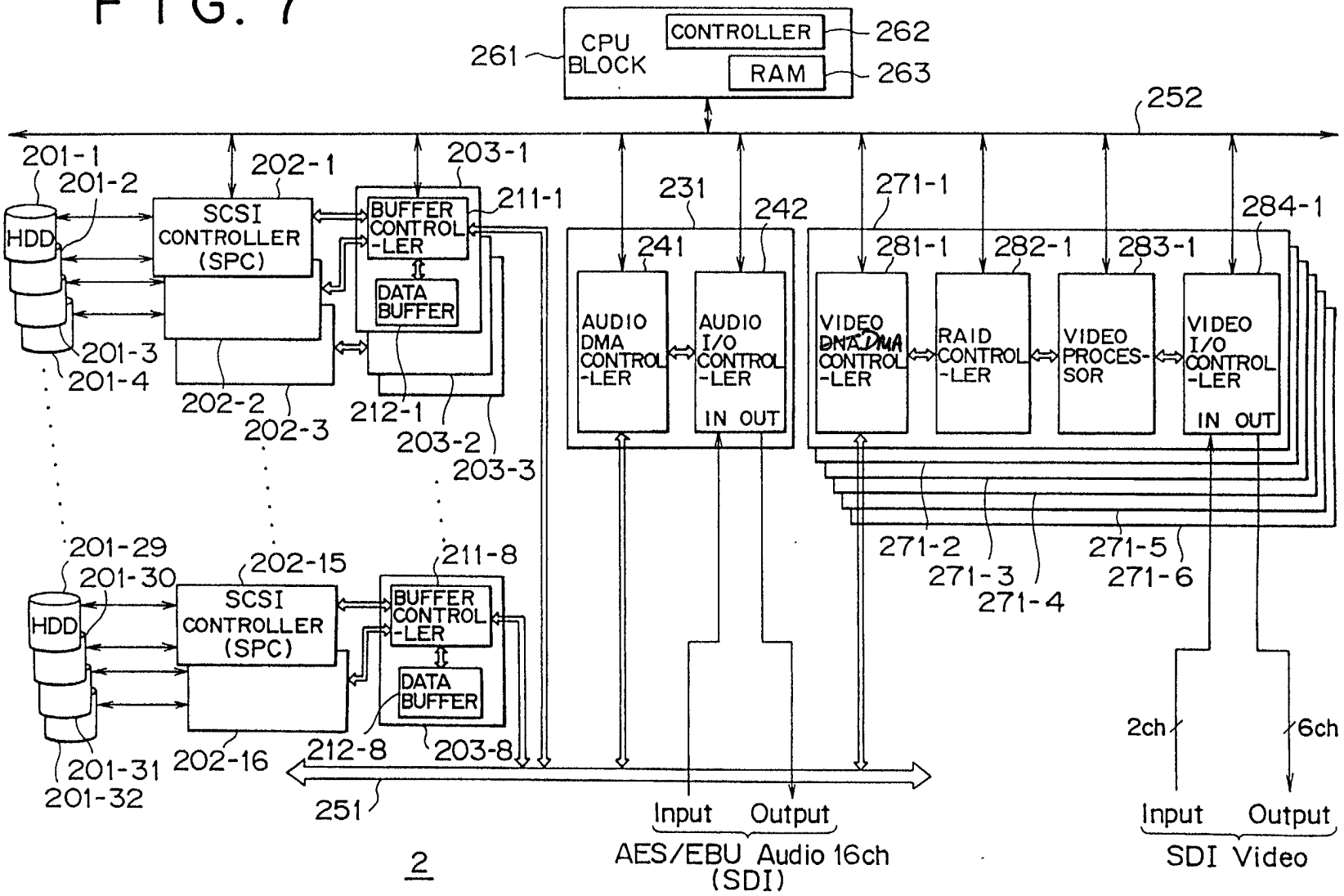

261
CPU BLOCK
CONTROLLER
262
RAM
263
252
201-1
201-2
202-1
203-1
211-1
231
242
271-1
284-1
241
281-1
282-1
283-1
HDD
SCSI CONTROLLER (SPC)
BUFFER CONTROL -LER
DATA BUFFER
AUDIO DMA CONTROL -LER
AUDIO I/O CONTROL -LER
IN OUT
VIDEO DMA CONTROL -LER
RAID CONTROL -LER
VIDEO PROCES-SOR
VIDEO I/O CONTROL -LER
IN OUT
201-3
201-4
202-2
202-3
212-1
203-2
203-3
271-2
271-3
271-4
271-5
271-6
201-29
201-30
202-15
211-8
201-31
201-32
202-16
212-8
203-8
251
2ch
6ch
Input
Output
AES/EBU Audio 16ch (SDI)
Input
Output
SDI Video
2

FIG. 11A

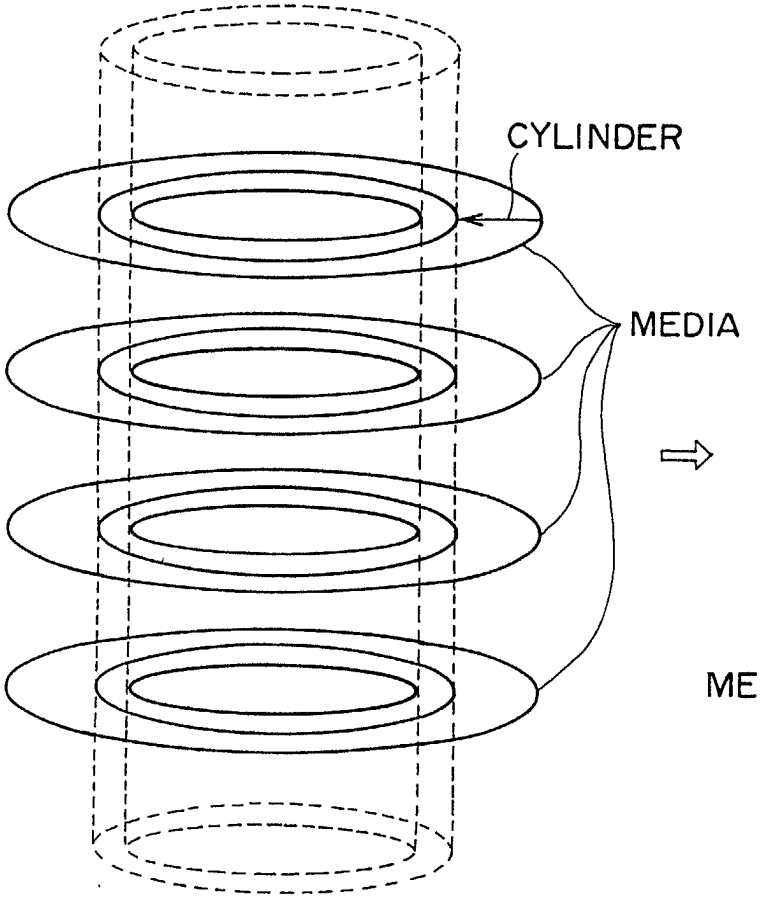


FIG. 11B

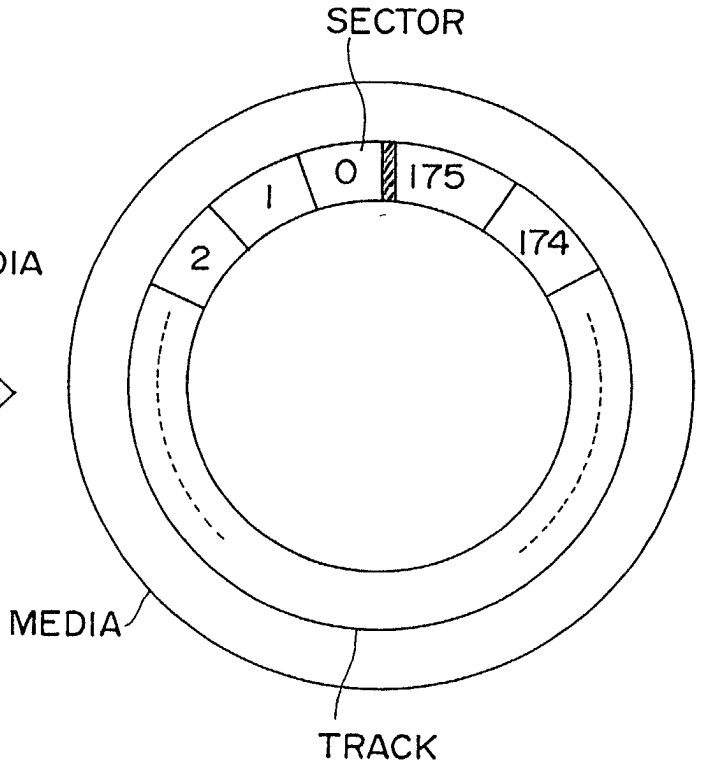


FIG. 16

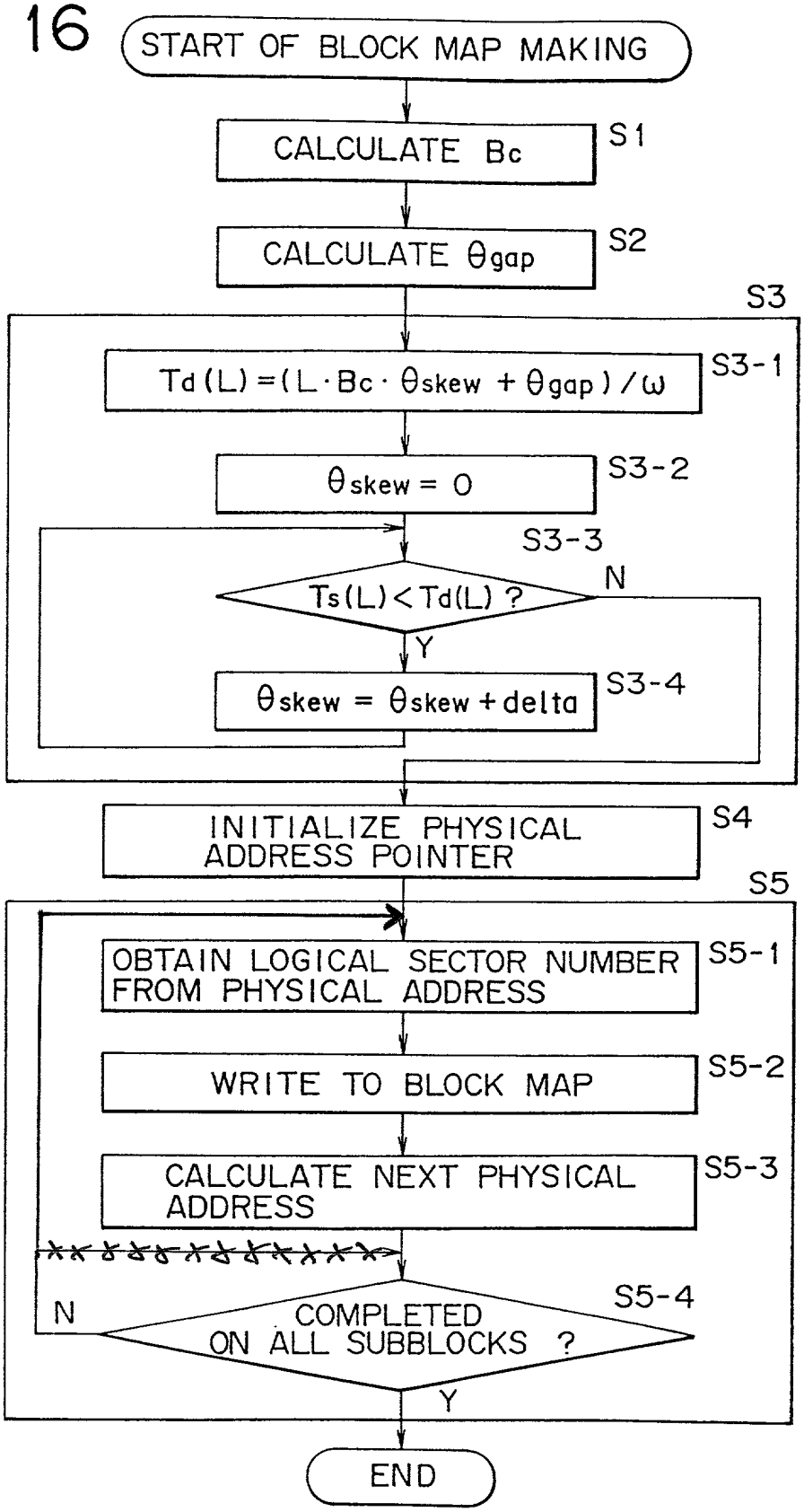

START OF BLOCK MAP MAKING
CALCULATE Bc
S1
CALCULATE θgap
S2
S3
Td(L) = (L · Bc · θskew + θgap) / ω
S3-1
θskew = 0
S3-2
S3-3
Ts(L) < Td(L) ?
N
Y
θskew = θskew + delta
S3-4
INITIALIZE PHYSICAL ADDRESS POINTER
S4
S5
OBTAIN LOGICAL SECTOR NUMBER FROM PHYSICAL ADDRESS
S5-1
WRITE TO BLOCK MAP
S5-2
CALCULATE NEXT PHYSICAL ADDRESS
S5-3
N
COMPLETED ON ALL SUBBLOCKS ?
S5-4
Y
END

FIG. 17

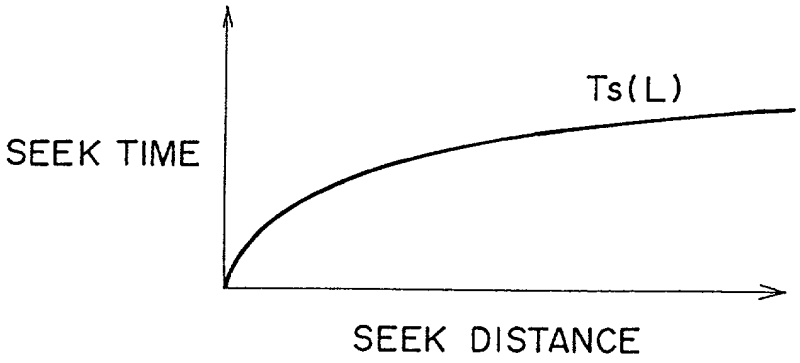

Ts(L)
SEEK TIME
SEEK DISTANCE

FIG. 18

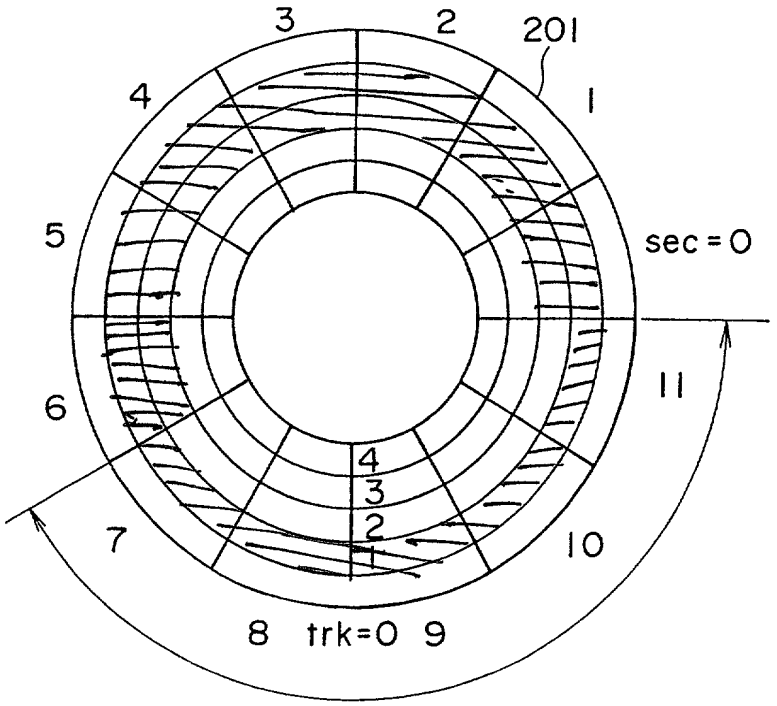

3
2
201
1
4
5
sec=0
6
11
4
3
2
1
7
10
8
trk=0
9

FIG. 19

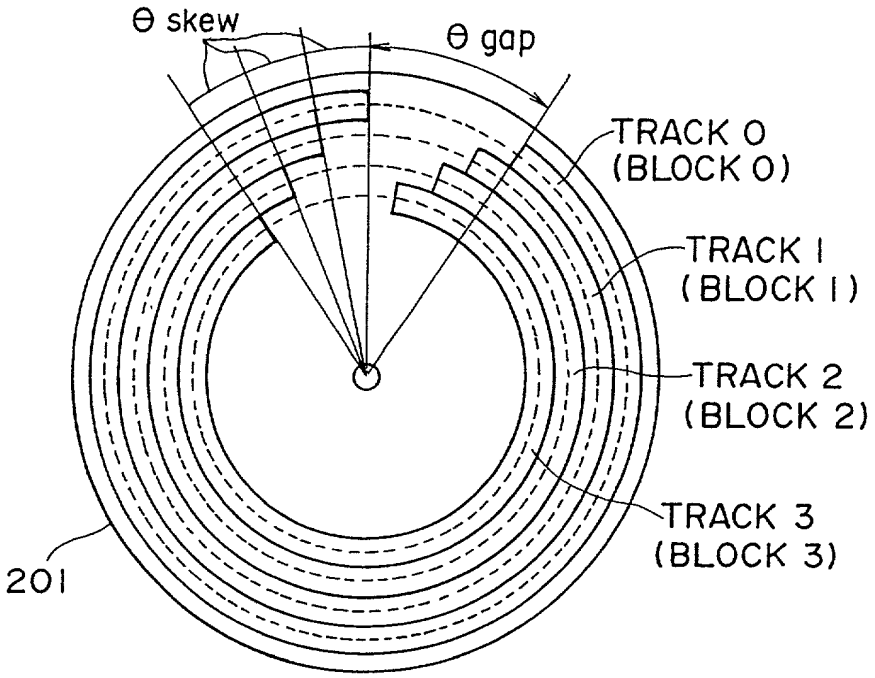

θ skew
θ gap
TRACK 0
(BLOCK 0)
TRACK 1
(BLOCK 1)
TRACK 2
(BLOCK 2)
TRACK 3
(BLOCK 3)
201

FIG. 20

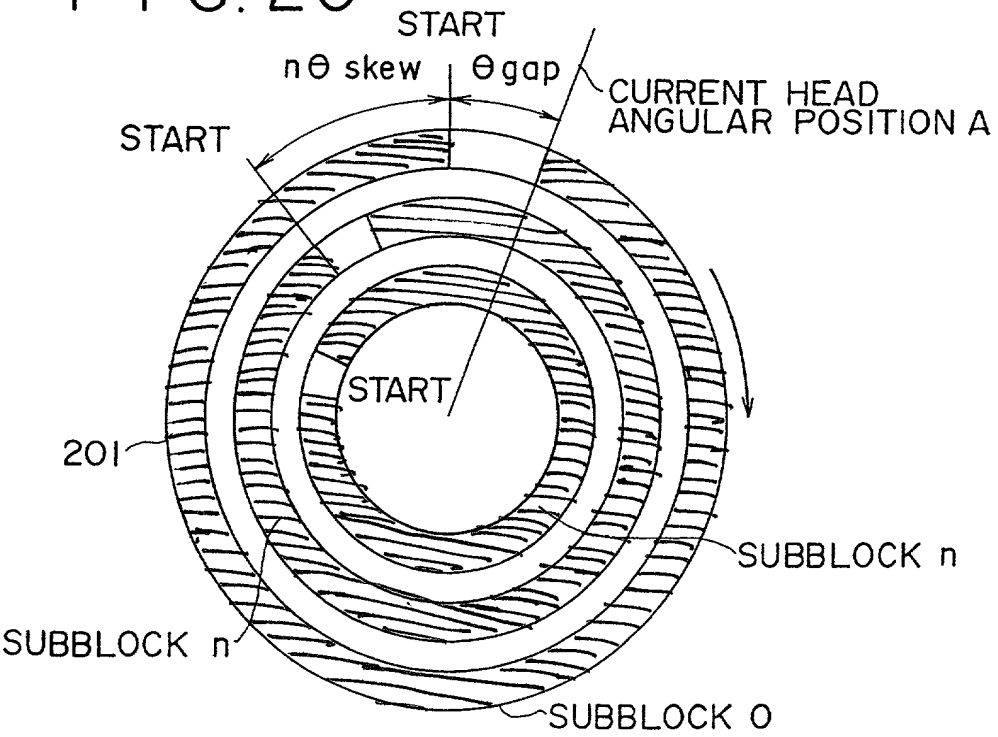

START
nθ skew
θ gap
CURRENT HEAD
ANGULAR POSITION A
START
START
201
SUBBLOCK n
SUBBLOCK n
SUBBLOCK 0

FIG. 33

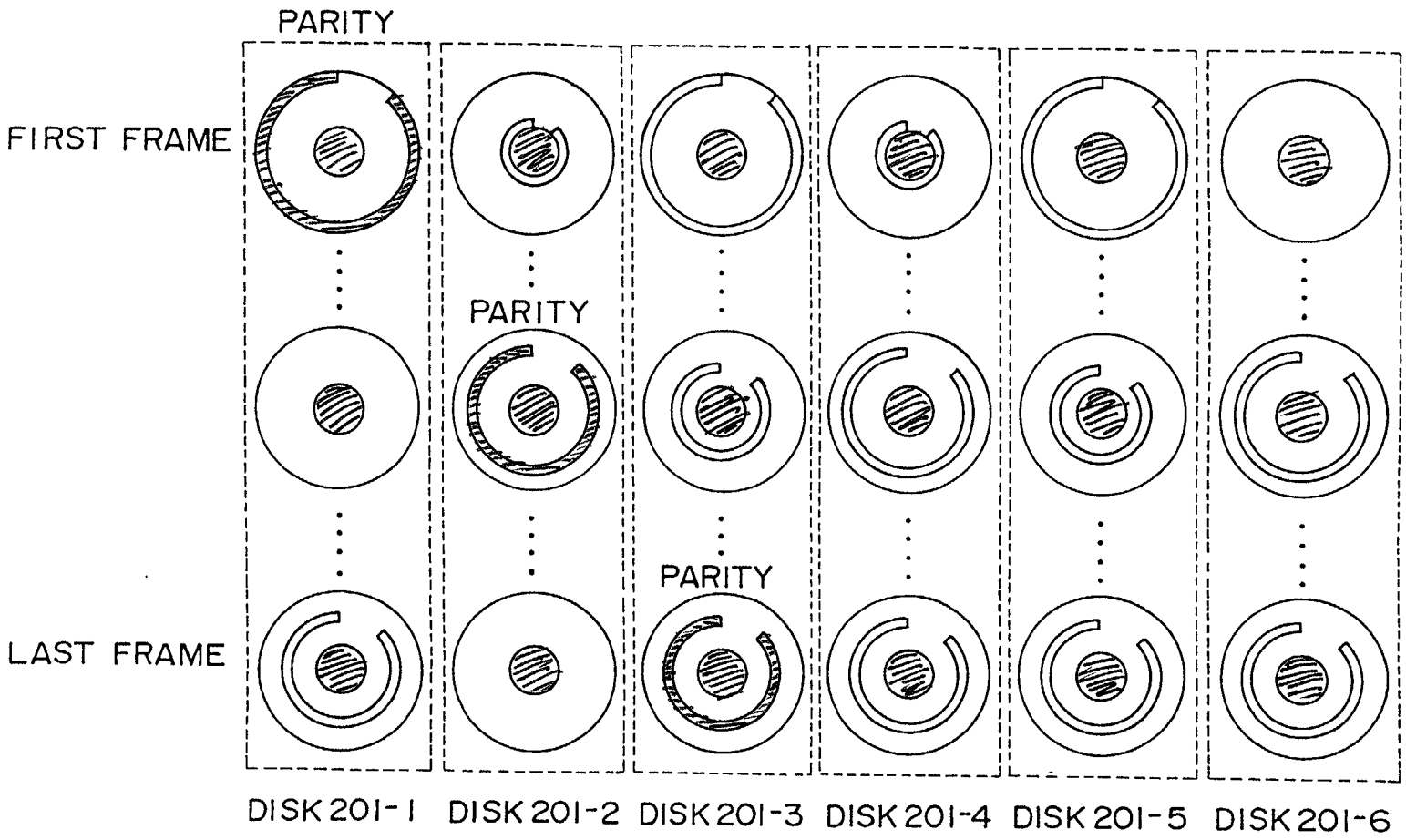

PARITY
FIRST FRAME
PARITY
PARITY
LAST FRAME
DISK 201-1
DISK 201-2
DISK 201-3
DISK 201-4
DISK 201-5
DISK 201-6

FIG. 48

DATA NUMBER (PACKET ~~TRASFER~~ TRANSFER BLOCK)	0	1	2	3	4	5	6	...
SELECTOR 451	A	A	A	A	A	A	A	
SELECTOR 455	A	A^B	A^B	A^B	A	A^B	A^B	
INPUT DATA	0	1	2	3	4	5	6	
DELAY ELEMENT 403	0	0^1	0^1^2	0^1^2^3	4	4^5	4^5^6	
PARITY DATA OUTPUT	0	0^1	0^1^2	0^1^2^3	4	4^5	4^5^6	

PARITY TO BE FOUND (under column 3)

PARITY GENERATION

FIG. 54

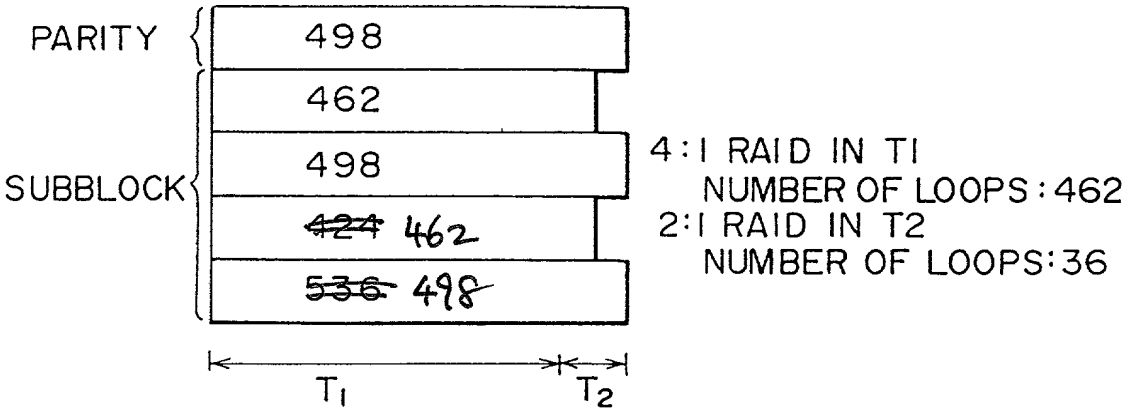
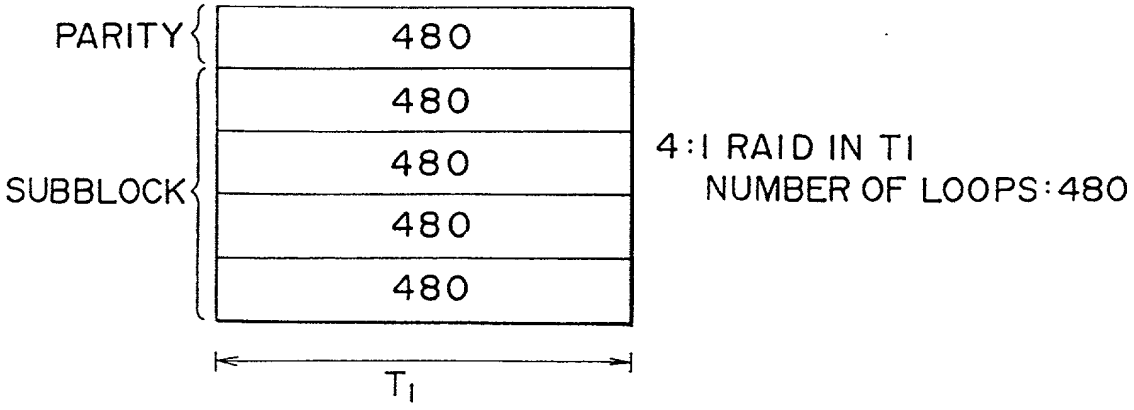

PARITY
SUBBLOCK
498
462
498
~~424~~ 462
~~536~~ 498
4:1 RAID IN TI
NUMBER OF LOOPS:462
2:1 RAID IN T2
NUMBER OF LOOPS:36
T1
T2

FIG. 55


PARITY
SUBBLOCK
480
480
480
480
480
4:1 RAID IN TI
NUMBER OF LOOPS:480
T1

F I G. 62B

4	5	6
S1 3(INNER)	S1-4(OUTER)	
S2 2(OUTER)	S2-3(INNER)	S2-4(OUTER)
S3 1(INNER)	S3-2(OUTER)	S3-3(INNER)
P4 (OUTER)	S4-1(INNER)	S4-2(OUTER)
	P5 (OUTER)	S5-1(INNER)
S6 4(OUTER)		P6 (OUTER)
S7 3(INNER)	S7-4(OUTER)	
S8 2(OUTER)	S8-3(INNER)	S8-4(OUTER
S9 1(INNER)	S9-2(OUTER)	S9-3(INNER)
P10 (OUTER)	S10-1(OUTER)	S10-2(OUTER)
⋮	⋮	⋮